DESIGN AND DEVELOPMENT OF DIGITAL I/Q MODULATOR

S. G. Kulkarni, J. A. Gore, A. K. Gupta, P. V. Bhagwat, R. K. Choudhury, BARC, Mumbai, India

Abstract

The control of RF cavity amplitude and phase is mostly done using analog I/O modulators. I and Q are rectangular coordinates of a sine wave which are used for calculating amplitude and phase of an RF signal. This paper presents a digital technique for modulator implementation using an FPGA.

The technique implemented uses look-up tables to store values of I and Q for different amplitudes/phase of RF signal. Using direct digital synthesis (DDS) block inside the FPGA, I/O data is converted into digital RF signal of pre-determined amplitude and phase which is given to high speed DAC which converts it into analog RF signal. The frequency, amplitude and phase of the required RF signal are easily changed by changing the I/Q values in the look-up tables and parameters o DDS block. The digital technique is flexible, accurate and less sensitive to aging and temperature effects compared to analog components. The technique is used for closed loop control of RF cavities as well as linearization of RF power amplifiers.

THEORY OF I/Q MODULATION

Figure 1 describes the basic decomposition of any sine/cosine signal. I and Q are nothing but rectangular coordinates of a periodic sine/cosine waveform. The conversion of I and Q into polar coordinates (Amplitude and phase) is explained in the following equations.

$$y(t) = A.\sin(\omega t + \varphi) \quad (1)$$

Using sin (A + B) formula we get

$$y(t) = A.\sin(\omega t).\cos(\varphi) + A\sin(\varphi).\cos(\omega t) \quad (2)$$

Rearranging the terms of equation 2, we get

$$y(t) = \underbrace{A.\cos(\varphi)}_{\mathbf{I}}\sin(\omega t) + \underbrace{A\sin(\varphi)}_{\mathbf{Q}}.\cos(\omega t) \quad (3)$$

I: In Phase component
Q: Quadrature phase component

$$y(t) = I.\sin(\omega t) + Q.\cos(\omega t) \quad (4)$$

$$I = A.\cos(\varphi)$$
$$Q = A.\sin(\varphi)$$

$$A = \sqrt{I^2 + Q^2} \quad (5)$$

$$\varphi = \tan^{-1}\left(\frac{Q}{I}\right) \quad (6)$$

Where A = Amplitude of the signal and
Φ = phase of the signal.

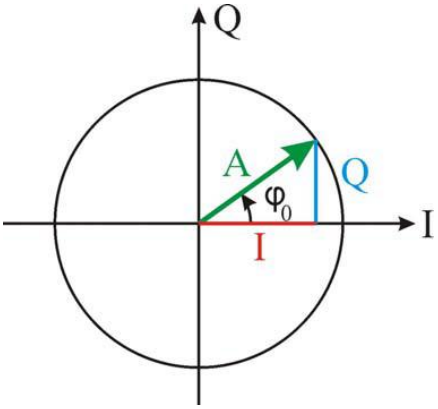

Figure 1: Decomposition of I and Q of a signal

BLOCK DIAGRAM DESCRIPTION

Figure 2 describes the basic block diagram of I/Q modulator. A DAC (which is external to FPGA) is used in the system for converting digital output into analog waveform. The basic building blocks used in the FPGA are:

a. DDS (Direct Digital Synthesis).
b. 18x18 Multiplier.
c. 20 bit adder.
d. LUT (Look-up-Tables).

The DDS block is used to generate sine and cosine waveforms simultaneously as they are required to be multiplied with I and Q respectively. The clock frequency for the DDS block is 125 MHz which is kept same as DAC clock frequency so that there is no mismatch between them and no sample is missed by the DAC while conversion. The maximum output frequency which is generated by I/Q modulator is restricted to 5 MHz considering the maximum conversion speed of DAC without distortion. DDS block implemented in the Xilinx Virtex-5 FPGA is configurable for output frequency and phase. In this application the frequency of the DDS is selected by the required RF frequency (restricted to maximum of 5 MHz).

The 18x18 multiplier block is available in the Virtex-5 FPGA which can be used for multiplication of I with sine output of DDS and Q with cosine output of DDS. Hence two multiplier blocks are required for this application. An adder just adds the two multiplied outputs coming out of two multipliers. Finally the result is truncated to 14 bits as the DAC resolution is 14 bits.

LUTs are used to store different I and Q values which are required to generate different frequencies/phase. I and Q will decide the amplitude of the output RF signal. To

have constant RF phase with change in amplitude, both I and Q should be equal. Both should be increased /decreased simultaneously to avoid any changes in the phase of the RF output.

The Iref and Qref inputs at the input section of I/Q modulator are used for setting the reference amplitude/phase of the RF output. Any subsequent changes to these values can be made dynamically by varying I and Q inputs which are internally subtracted from Iref and Qref respectively.

FPGA BOARD DESIGN

The Virtex-5 FPGA board used for this application had two DAC channels and two ADC channels. The ADC channels were introduced for closed loop applications where there is a need to monitor amplitude and phase of RF signal and then correct I and Q values of I/Q modulator. The board has 125 MHz clock generator along with other power supplies and SMA connectors. This mixed signal 8 layered board is designed with proper grounding techniques which are necessary when both ADC/DAC and FPGA are together on-board.

CONCLUSION AND APPLICATIONS

I/Q modulator is tested by controlling a RF amplifier and RF input to the amplifier is easily changed by changing I and Q values. This digital technique is flexible, accurate and less sensitive to aging and temperature effects compared to analog components.

The technique is used for closed loop control of RF cavities as well as linearization of RF power amplifiers.

REFERENCES

[1] Xilinx Virtex-5 User Guide.

[2] CARTESIAN FEEDBACK FOR RF POWER AMPLIFIER LINEARIZATION (Joel L. Dawson and Thomas H. Lee), Center for Integrated Systems, Stanford University

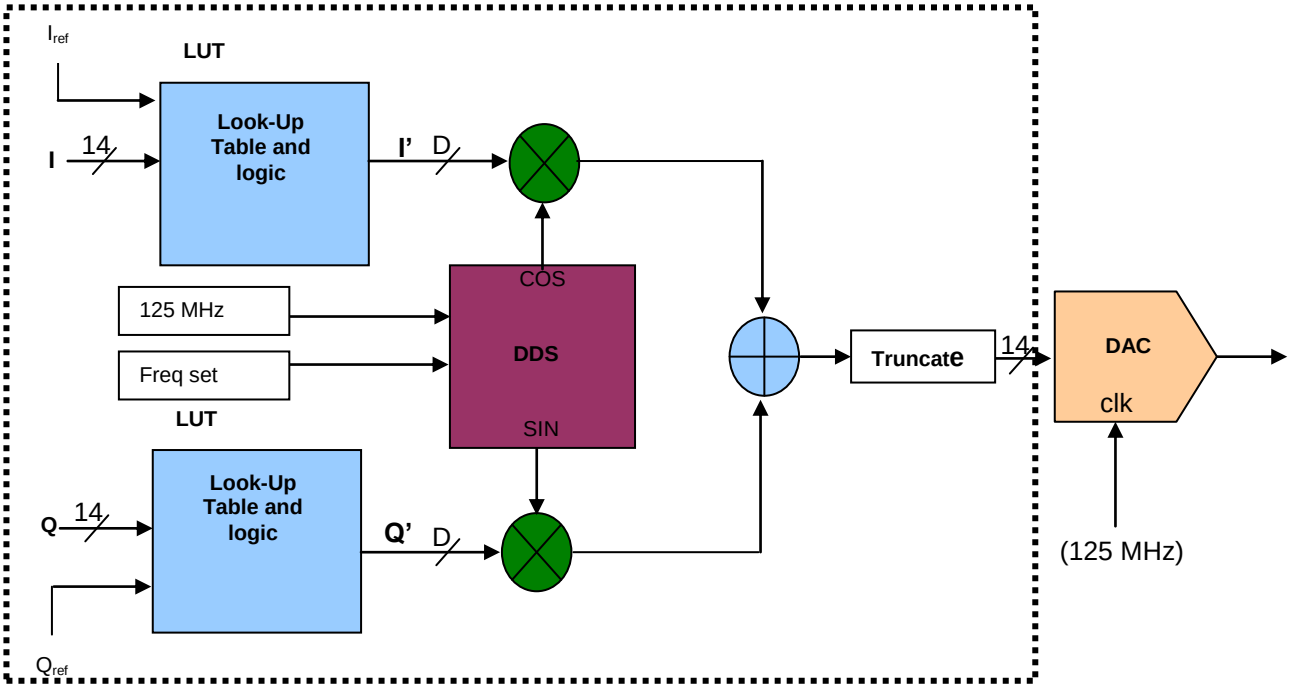

Figure 2: Block diagram of I/Q Modulator (Dashed line indicates the logic inside FPGA)