FPGA BASED 8 CHANNELS 4K ANALOG TO DIGITAL CONVERTER

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Abstract

FPGA based high precision pulse peak detection, analog to digital converter (ADC) suited for spectroscopy experiments has been designed and developed. This is a single width CAMAC module, which includes 8 independent channels of 12-bit resolution analog to digital converters in plug-in daughter card motherboard model and exhibiting very good integral non-linearity (INL) of ≤ ±0.05% and differential non-linearity (DNL) of ≤ ±0.02LSB over 10% to 90% of range. It was designed, developed and tested, in house and gives the advantage of cost effective and ease of maintenance.

INTRODUCTION

Output from various detectors is mostly in the form of electrical analog signals. When it is desired to have very precise and accurate measurement, it is almost imperative to transform the analog signals into proportional digital numbers. Once the data are available in digital form, all the modern digital techniques of data are available in digital readout and transmission etc, can be gainfully employed. An electronic device which performs the conversion of analog signals into digital form in a linear relationship is known as Analog to Digital Converter or simply ADC. Of the different types of ADC's, the 'Wilkinson' type ADC have high resolution and good linearity but very large conversion time, of the order of 80 µs. On the other hand high speed flash ADCs are very fast with a compromise between resolution and linearity. The trade off between these two is to use easily available high speed successive approximation ADCs, in combination with the sliding scale technique. This can provide almost the same results as that of 'Wilkinson' ADCs with less conversion time. This paper will give the details of design and development of FPGA based 8 channels 4K analog to digital converter CAMAC module which will be used for spectroscopy applications.

CIRCUIT DESCRIPTION

The ADC module was designed around a successive approximation ADC due to advantages mentioned in the introduction. AD977BRZ serial ADC chip from Analog Devices is used because of its compact package and good linearity. The value of DNL as per specification was ≤ ± 2 LSBs. The requirement for the spectroscopy application was ≤ ± 1%, and therefore a sliding scale DNL correction technique has been implemented. The individual ADCs along with peak detection and stretch circuits are integrated on daughter cards. The daughter cards plug into a mother board through spring loaded gold plated contacts. The motherboard implements the communication to the daughter cards, front panel indicators and the CAMAC back plane interface.

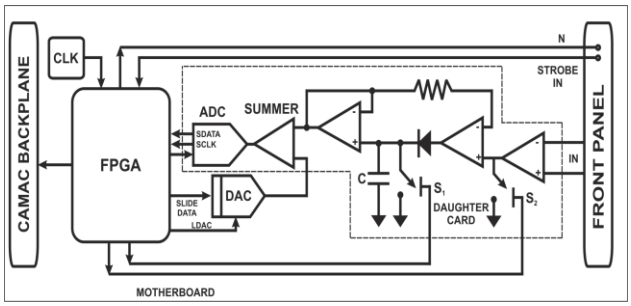


Figure 1: Block diagram of ADC module

Motherboard

The mother board takes care of the communication with each individual ADC, the CAMAC back plane interface and provides the triangular ramp for the sliding scale digital to analog converter (DAC) which is common to all the ADC daughter cards. It also receives and process the strobe input, drives the 'N' indicator LED on the front panel. The central core of the module is the Xilinx 4010EPQ FPGA, which is programmed in 'VHDL' to provide the back plane interface and necessary timing and control for analog and digital circuits. The data from the ADCs are simultaneously collected and stored in the FPGA through the two wire serial communication provided by the ADC chip. Analog conversion is enabled and initiated by a strobe input (Negative NIM) that is common to all the channels.

Figure 2: Inside view of ADC module

Sliding scale

The differential non-linearity of the successive approximation type ADC is worse than that of Wilkinson ADC. However, we have implemented the sliding scale technique, to achieve better DNL. A digital to analog converter (DAC) with good linearity and monotonicity

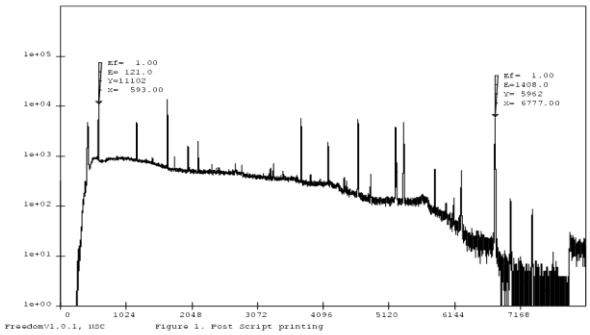
(AD569KN from Analog Devices, with a guaranteed monotonicity and linearity of ≤ ± 0.25 LSB typ) was chosen to provide the sliding scale voltage. A seven bit up down counter clocked at the end of every acquire cycle is given as input to the digital to analog converter. The DAC provides the corresponding analog triangular waveform that changes in value between the ADC conversions. This output of the DAC is added to the input signal before the start of digitization. After the analog signal is digitized, the counter is incremented and consequently the DAC is set to the next value in preparation for the next pulse, thereby ensuring sufficient settling time for the DAC. The pulses arriving at the input have a random distribution in sliding scale values providing a better DNL. The analog slide voltage thus added is then subtracted out digitally from the digitized value. The sliding scale generator is common to all the eight channels. The addition of a sliding voltage to the input signals of the same amplitude are converted on 128 consecutive channels of the ADC, thereby averaging the DNL error over a range of 128 channels. But the use of the sliding scale equivalent to 128 channels (i.e., 7 bits) reduces the dynamic range of the maximum measurable signal by the ADC from 4095 channels to 3967 channels. A jumper on the motherboard will enables the sliding scale circuit.

Daughter cards

The daughter card consists of a serial ADC, sliding scale summer, peak detection and peak stretch, input differential amplifier. The analog input is fed to a differential input front end amplifier will help to avoid the ground loop differences in different detectors and their corresponding shaping amplifiers. An active rectifier with peak detect and stretch circuit is used to detect and store the peak height of the input pulse. The differential input is converted into a single ended signal and fed to the peak detect and stretch section. Peak detect and peak stretch cycles are started with the strobe pulse. Strobe input enables the peak detection circuit and the peak of the incoming analog pulse is stored by charging the 'Hold capacitor' through an active rectifier. When the strobe input is not asserted, the input signal is disconnected from the peak detection section. This way the voltage across the peak hold capacitor remains unaffected to changes in the input signal beyond the strobe. Low drooping is achieved by the selection of appropriate operational amplifiers with very low input bias currents. After conversion and acquiring cycles are finished, 'Hold capacitor' is reset and maintained at zero by the low 'true' peak stretch signal till the start of next conversion cycle.

A successive approximation ADC with a 8 µs conversion time and better inherent non linearity with guaranteed (as specified by the analog devices data sheet for the ADC chip being used and also verified in the test process) no missing codes was verified. With this the amount of time taken to read all the channels remains the same independent of number of inputs present. The serial clock running at 10 MHz is used as the synchronization clock (SCLK) for reading the ADC data and it takes about 3.4µs. The serial data from the ADCs are collected simultaneously through 8 different I/O pins of the FPGA into respective serial shift registers. This is achieved in 3.4µs. The start of conversion ('SOC') signal for the ADC is also asserted not just immediately after the end of strobe input, but after a delay of 100 ns. This avoids any switching noise caused due to strobe crept into the peak stretch circuit getting digitized. Practically the entire module comes to hold mode (for ≈ 8 µs) till the busy of the ADC is de asserted. This also led to chose 'external discontinuous clock data read after conversion' mode for reading data from the serial ADCs, as in this method the conversion performance is not degraded as the data is not clocked out during conversion.

Figure 3: ADC output with EU152 Source



CONCLUSION

We have designed and fabricated a FPGA based 8 Channels 4K analog to digital converter module suitable for use in spectroscopy and particle physics experiments. Individual ADCs on daughter cards are based on a design without multiplexing and with a conversion time of 12.4 µs. An integral linearity of ≤ ±0.05% and differential non-linearity of ≤ ±0.02LSB were observed during in house testing. As it is indigenously developed, it ensures ease of maintenance and as well the production cost is reduced to great extent.

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