IMPROVEMENTS IN INDUS TIMING CONTROL SYSTEM AND EXPERIENCE WITH FPGA BASED DELAY GENERATOR BOARDS

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Abstract

Timing control systems (TCS) of Indus Accelerator Complex play an important role for successful beam injection from booster ring into storage rings (Indus-1 and Indus-2). Apart from giving reference current amplitude settings, TCS also generate precisely delayed triggers for injection and extraction magnet pulsed power supplies. TCS of the two rings are now equipped with recently developed FPGA based delay generator boards. Indus-2 TCS is upgraded to generate Indus-2 bunch revolution clock while Indus-1 TCS is upgraded to accommodate booster extraction interlocking requirement and add diagnostic features to control beam extraction etc. The revolution clock signal, locked with Indus-2 RF clock, adds to diagnostic tools for understanding bucket filling patterns. Interlocking beam extraction from booster is compulsory now from radiation safety point of view. This paper describes the particular technique used to generate revolution clock. Paper also discusses the efforts made for improved performance and smooth round the clock operation and highlights the advantages gained from use of FPGAs in above mentioned efforts.

INTRODUCTION

Timing control systems for Indus-1 and Indus-2 are responsible for generating precisely delayed trigger signals for pulsed power supplies (PPS) of booster beam injection/extraction [2] and Indus-1 (or Indus-2) injection kicker & septum magnets. Indus-2 is designed to have 291 buckets to accommodate injected bunches. This is achieved by generation of coincidence clock of booster and Indus-2 RF clocks. Proper rate of injection in Indus-1 or Indus-2 depends critically on preciseness of these triggers and coincidence clock in addition to other governing factors.

ENHANCEMENTS IN INDUS-2 TCS

Revolution Clock generation

With the in-house development and deployment of FPGA based coincidence clock generator VME boards [1] for Indus-2 TCS, it became easy to fulfil any enhancement requirement as and when needed for machine studies. One such requirement was to provide bunch revolution clock signal locked with Indus-2 RF clock. The revolution clock of Indus-2 is governed by the following relation

$$F_{Rev} = F_{I\text{-}2RF}/291$$

Where, $F_{I\text{-}2RF}$ is Indus-2 RF clock (505.8MHz). Generating this revolution clock was not as straight as it seems because the input to the coincidence clock generator board is $F_{Inp} = F_{I\text{-}2RF}/8$ (~ 63.23MHz), which comes from clock divider ECL (Emitter Coupled Logic) circuit. So effectively

$$F_{Rev} = (8/291)*F_{Inp} = (8/3*97)*F_{Inp}$$

To generate this revolution clock, F_{Inp} is first divided by 3 and multiplied by a factor of 8 to generate intermediate clock signal of frequency 168.6MHz. This is done using frequency synthesizer of Digital Clock Manager (DCM) [4] of on-board XC3S50-4VQ100 FPGA from Xilinx [3]. DCM is a clock management soft IP core that provides multiple functions. It can implement a clock delay locked loop, a digital frequency synthesizer, digital phase shifter, and a digital spread spectrum. Then this intermediate clock was divided using counter of mod 97 to generate exact F_{Rev} (1.738MHz) locked with Indus-2 RF clock. F_{Rev} clock signal is presently provided in control room through trigger transfer unit (TTU) from Indus-2 TCS VME station. This is used with Transport Line-3 (TL3) & Indus-2 Wall Current Monitor (WCM) signals to analyze individual bucket filling patterns during injection.

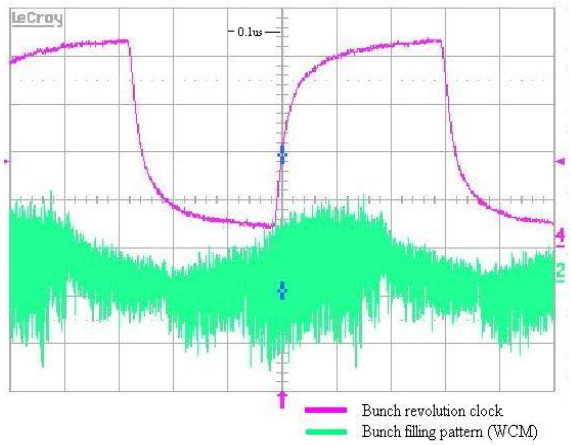

Figure 1 Indus-2 bucket filling pattern with revolution clock

This analysis helps to observe irregularity in bucket filling pattern if any and identifying fast decaying buckets. Figure 1 shows the plot of bunch filling pattern (green) with revolution clock (pink). The revolution clock signal is also proposed to be used in new BPM digital front end system, which is being evaluated for experiments on turn by turn beam position measurements.

Coarse delay generator board

Two 2-channel old delay generator boards were replaced with recently developed one, 5-channel FPGA based coarse delay generator board. Earlier Indus-2 TCS VME station made use of total nine VME boards with six coarse delay generator boards, two fine delay generator boards, one coincidence clock generator board and one interrupt generator board. Present Indus-2 TCS VME station after upgrading with FPGA based delay generator boards, employs total of five VME boards. It is also proposed to design new coincidence clock generator board with interrupt generation logic integrated on it.

MODIFICATIONS IN INDUS-1 TCS

'Permission to extract' trigger generator boards

'Permission to extract' trigger is the first trigger generated at Indus-1 TCS for Indus-1 and Indus-2 injection, with respect to which, all other delayed triggers for related Pulsed Power Supplies (PPS) are generated. These signals are generated at flat top of booster ramp with different delays for injection in Indus-1 and Indus-2. These delays are related to beam extraction at two different energy levels of 450 MeV for Indus-1 and 550Mev for Indus-2. Considering the successful and fruitful experience of deploying FPGA based delay generator boards in Indus-2 TCS, one FPGA based 5-channel coarse delay generator board was deployed in Indus-1 TCS to replace one 4-channel delay generator board. VHDL code for the FPGA (XC3S50-4VQ100) was modified to fit here and fulfil the immediate requirement of stopping the extraction of beam from booster during interlock fail condition. This condition was imposed recently from radiation safety concerns arising because of unwanted beam extraction during user's presence in Indus-1 area. These changes were augmented with some hardware changes to have room for interlock status signal and mode of operation signal (Indus-1 or Indus-2 filling mode, one at a time). Following these modifications, further enhancements were done to provide 'permission to extract' signal in diagnostic mode bypassing interlock status and mode of operation for testing and debugging purpose during PPS related maintenance activities. Permission to extract signal in diagnostic mode was generated to ensure that it does not result in beam extraction from booster. This was done by delaying this trigger by 830 ms to ensure that it comes after booster ramp cycle has completely vanished. This was necessary to ensure that no beam is extracted from booster during diagnostic mode. Indus-1 TCS GUI panel is also modified to display diagnostic information in control room.

Coarse-fine delay generator board for Indus-1

Recently, one 5-channel FPGA based coarse-fine delay generation VME board is deployed for setting delays for beam injection in Booster synchrotron. Prior to this, separate coarse and fine delay generator boards were in existence. Previous boards were designed long back with the help of the then available electronics. Some parts of the circuit were not synchronous to the concerned on-board clock with the view to achieve the functionality with minimum components to reduce unwanted delays. Latest FPGA based board takes care of it. Over all, most of the logic functionality is implemented into single chip, which helps in achieving the defined delay of the order of nanosecond which is little difficult to achieve by using discrete components on a PCB.

FUTURE PLANS AND RELATED ACTIVITIES

It is proposed to upgrade the existing Indus-1 timing control system. This will involve proposal of new control architecture and development of new circuit boards. Based on experience gained, in addition to development of enhanced version of the delay generator boards, it will be required to provide several diagnostic features. Diagnostic features will help to certify the wellness of generated triggers in control room, eliminating the need to visit equipment control station when the system is doubted for its wellness. Work on development of new version of FPGA based delay generator boards with many diagnostic features is in hand. Optical fibre based isolation between Equipment control layer and equipments (high power pulsed power supplies) will also be emphasized in proposed scheme.

REFERENCES

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